What is claimed is:

1. A method of etching a silicon nitride film comprising:

forming a buffer layer of silicon dioxide on a semiconductor substrate;

forming a silicon nitride film on the buffer layer;

heating the semiconductor substrate to a process temperature of at least about 40 °C; and

etching the silicon nitride film using a plasma generated from an etching gas including CH_2F_2, while maintaining the semiconductor substrate at the process temperature.

2. The method of etching a silicon nitride film according to claim 1, wherein:

the etching gas further includes CF_4.

3. The method of etching a silicon nitride film according to claim 1, wherein:

the etching gas further includes argon.

4. The method of etching a silicon nitride film according to claim 1, wherein:

the etching gas further includes O_2.

5. The method of etching a silicon nitride film according to claim 1, wherein:

the etching gas includes a mixture of CH_2F_2, Ar and one gas selected from a group consisting of CF_4 and O_2; and further wherein;

the plasma etches silicon nitride at a first etch rate;

the plasma etches silicon dioxide at a second etch rate; and

a ratio of the first etch rate to the second etch rate is at least 5:1.

6. The method of etching a silicon nitride film according to claim 1, wherein:

the process temperature is between about 60 and about 100 °C.

7. The method of etching a silicon nitride film according to claim 1, wherein:

etching the silicon nitride film includes:

loading the semiconductor substrate on which the silicon nitride film has been formed onto a supporting plate within an etching chamber;

heating the semiconductor substrate to the process temperature by heat transfer from the supporting plate; and

introducing the etching gas into the etching chamber and applying RF power to the etching gas to form the plasma within the etching chamber.

8. A method of manufacturing a semiconductor device comprising:

forming a gate insulation film on a semiconductor substrate;

forming a gate structure having a gate electrode and a gate mask on the gate insulation film;

forming a first buffer layer including silicon oxide on the gate structure and on the semiconductor substrate;

forming a silicon nitride film on the first buffer layer;

heating the semiconductor substrate to a first processing temperature of at least about 40 °C;

forming a first plasma from a first etching gas including CH_2F_2; and

etching the silicon nitride film using the first plasma to form a gate spacer along a sidewall of the gate structure while maintaining the semiconductor substrate at the first process temperature.

9. The method of manufacturing a semiconductor device according to claim 8, wherein:

the first etching gas further includes CF_4.

10. The method of manufacturing a semiconductor device according to claim 8, wherein:

the first etching gas further includes argon.

11. The method of manufacturing a semiconductor device according to claim 8, wherein:

the first etching gas further includes O_2.

12. The method of manufacturing a semiconductor device according to claim 8, wherein:

the first etching gas includes a mixture of CH_2F_2, Ar and one gas selected from a group consisting of CF_4 and O_2; and further wherein;

the first plasma etches silicon nitride at a first etch rate;

the first plasma etches silicon dioxide at a second etch rate; and

a ratio of the first etch rate to the second etch rate is at least 5:1.

13. The method of manufacturing a semiconductor device according to claim 8, further comprising:

forming a second buffer layer on the gate structure, the gate spacer and the semiconductor substrate, the second buffer layer including silicon oxide;

forming an etch stop layer on the second buffer layer, the etch stop layer including silicon nitride;

forming an interlayer insulation film on the etch stop layer;

removing the interlayer insulation film from a contact hole region, thereby exposing a region of the etch stop layer;

heating the semiconductor substrate to a second process temperature of at least about 40 °C.;

removing the exposed region of the etch stop layer with a second plasma generated from a second etching gas that includes CH_2F_2 while maintaining the semiconductor substrate at the second process temperature thereby exposing a region of the second buffer layer; and

removing the exposed portion of the second buffer layer to expose a region of the semiconductor substrate and form a contact opening.

14. The method of manufacturing a semiconductor device according to claim 13, wherein:

the second etching gas includes a mixture of CH_2F_2, Ar and one gas selected from a group consisting of CF_4 and O_2; and further wherein;

the second plasma etches silicon nitride at a third etch rate;

the second plasma etches silicon dioxide at a fourth etch rate; and

a ratio of the third etch rate to the fourth etch rate is at least 5:1.

15. The method of manufacturing a semiconductor device according to claim 14, wherein:

the first etching gas and the second etching gas include substantially the same mixture of CH_2F_2, Ar and one gas selected from a group consisting of CF_4 and O_2.

16. The method of manufacturing a semiconductor device according to claim 14, wherein:

at least one of the first process temperature and the second process temperature is at least about 60 °C.

17. The method of manufacturing a semiconductor device according to claim 14, wherein:

both the first process temperature and the second process temperature are at least about 60 °C.

18. A method of manufacturing a semiconductor device comprising:

forming a gate insulation film on a semiconductor substrate;

forming a gate structure having a gate electrode and a gate mask on the gate insulation film;

forming a first buffer layer including silicon oxide on the gate structure and on the semiconductor substrate;

forming a silicon nitride film on the first buffer layer;

etching the silicon nitride using an etch method according to claim 1 to form a gate spacer along a sidewall of the gate structure;

forming a second buffer layer on the gate structure, the gate spacer and the semiconductor substrate, the second buffer layer including silicon oxide;

forming an etch stop layer on the second buffer layer, the etch stop layer including silicon nitride;

forming an interlayer insulation film on the etch stop layer;

removing the interlayer insulation film from a contact hole region, thereby exposing a region of the etch stop layer;

etching the exposed region of the etch stop layer using an etch method according to claim 1 to expose a region of the second buffer layer; and

removing the exposed portion of the second buffer layer to expose a region of the semiconductor substrate and form a contact opening.